What Is Claimed Is:

1. A method forming junction isolation to isolate active elements, comprising the steps of:

providing a semiconductor substrate having a plurality of active areas and at least one isolation area between any two active areas;

forming a first gate structure on part of the substrate located in the active areas and a second gate structure on the substrate located in the isolation area;

forming a first doped region in the substrate located at two sides of the first gate structure and two sides of the second gate structure;

forming a bottom anti-reflection layer on the substrate, the first gate structure and the second gate structure;

anisotropic etching back part of the bottom anti-reflection layer to expose the second gate structure;

removing the second gate structure to expose the surface of the substrate;

forming a second doped region in the substrate located in the isolation area, wherein a type of dopant in the first doped region is opposite to that in the second doped region; and

removing the bottom anti-reflection layer.

2. The method according to claim 1, wherein the first gate structure and the second gate structure are simultaneously formed on the substrate.

3. The method according to claim 1, wherein the second gate structure serves as a dummy gate structure.

4. The method according to claim 2, wherein the method of forming the first gate structure and the second gate structure comprises the steps of:

forming an insulation layer on the substrate;

forming a conductive layer on the insulation layer; and

anisotropic etching back part of the conductive layer and the insulation layer to form a gate layer and a gate insulation layer on the substrate.

5. The method according to claim 4, wherein the insulation layer is a SiO_2 layer.

6. The method according to claim 4, wherein the conductive layer is a polysilicon layer.

7. The method according to claim 1, wherein the first doped region is implanted with N-type ions and the second doped region is implanted with P-type ions.

8. The method according to claim 1, wherein the first doped region is implanted with P-type ions and the second doped region is implanted with N-type ions.

9. The method according to claim 1, wherein the anti-reflection layer is an organic layer.

10. A method of forming junction isolation to isolate active elements, comprising the steps of:

providing a semiconductor substrate having a plurality of active areas and at least one isolation area between any two active areas;

forming a first gate structure on part of the substrate located in the active areas and a second gate structure on the substrate located in the isolation area;

forming a first doped region in the substrate located at two sides of the first gate structure and two sides of the second gate structure;

forming a bottom anti-reflection layer on the substrate, the first gate structure and the second gate structure;

forming a patterned photoresist layer on the bottom anti-reflection layer located in the active areas;

using the patterned photoresist layer as a mask, anisotropic etching back part of the bottom anti-reflection layer to expose the second gate structure;

removing the second gate structure to expose the surface of the substrate;

forming a second doped region in the substrate located in the isolation area, wherein a type of dopant in the first doped region is opposite to that in the second doped region;

removing the patterned photoresist layer; and

removing the bottom anti-reflection layer.

11. The method according to claim 10, wherein the first gate structure and the second gate structure are simultaneously formed on the substrate.

12. The method according to claim 10, wherein the second gate structure serves as a dummy gate structure.

13. The method according to claim 11, wherein the method of forming the first gate structure and the second gate structure comprises the steps of:

forming an insulation layer on the substrate;

forming a conductive layer on the insulation layer; and

anisotropic etching back part of the conductive layer and the insulation layer to form a gate layer and a gate insulation layer on the substrate.

14. The method according to claim 13, wherein the insulation layer is a SiO_2 layer.

15. The method according to claim 13, wherein the conductive layer is a polysilicon layer.

16. The method according to claim 10, wherein the first doped region is implanted with N-type ions and the second doped region is implanted with P-type ions.

17. The method according to claim 10, wherein the first doped region is implanted with P-type ions and the second doped region is implanted with N-type ions.

18. The method according to claim 10, wherein the anti-reflection layer is an organic layer.